REMARKS

Careful review and examination of the subject application are noted and appreciated.

CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, FIGS. 1-3 and in the specification as originally filed, for example, on page 5, line 20 through page 9, line 2, on page 12, line 12 through page 13, line 2 and on page 13, line 12 through page 14, line 6. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-5, 7-13 and 15-24 under 35 U.S.C. §102(b) as being anticipated by New '834 (hereinafter New) is respectfully traversed and should be withdrawn.

New is directed to a field programmable gate array with distributed gate array functionality (Title).

In contrast, the presently claimed invention (claim 1) provides one or more logic circuits configured to provide logical operation where the one or more logic circuits comprise (i) programmable logic elements and (ii) **non-programmable hard wired blocks having no programmable elements** within a programmable logic

device. Claims 15 and 16 include similar recitations. New does not disclose or suggest a non-programmable hard wired block having no programmable elements, as presently claimed (see paragraph nos. 8 and 9 in the Declaration of Michael T. Moore). Therefore, New does not disclose or suggest each and every element of the presently claimed invention arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, the position taken in the Office Action that the Sea-of-Gates (SOG) gate array 203 of New is similar to the presently claimed non-programmable hard wired blocks having no programmable elements is not technically correct (see paragraph nos. 12 and 13 in the Declaration of Michael T. Moore). Furthermore, New states that the sea of gates (SOG) gate arrays are programmable. For example, the Abstract of New provides:

> . . . The non-field programmable gate array can be used to provide a plurality of mask-programmable input/output driver circuits for connection to the pads of the FPGA (Abstract of New, emphasis added).

New further states that:

> In an SOG gate array, a predefined pattern of transistors are connected directly with user-defined metal [i.e., mask-programmed], both to form gates and to interconnect those gates (column 1, lines 45-47 of New).

Further reference is made by New to the programmability of the SOG gate arrays, for example, in column 2, lines 12-14:

> . . . a corresponding non-field programmable gate array, such as a mask programmed gate array, or more specifically a sea-of-gates (SOG) gate array (emphasis added);

in column 8, lines 16-18:

> As described in more detail below, the SOG gate array 601 can be mask-programmed to implement an input and/or output driver circuit 615 which is coupled to the I/O pad 602 (emphasis added);

and in column 8, lines 36-44:

> The SOG gate array 601 includes logic elements which can be programmed to vary the composition of the input buffer 621 and the output buffer 622 (emphasis added).

Since the sea of gates array of New includes logic elements which can be programmed, it follows that New does not disclose or suggest a non-programmable hard wired block having no programmable elements, as presently claimed.

Furthermore, the Office Action does not present any evidence or line of reasoning supporting the position that one of ordinary skill in the art would view the mask-programmed gate array of New as being the same as a non-programmable hard wired block, as presently claimed. Furthermore, the Office has previously admitted that a hard wired circuit is not programmable:

> . . . if the logic circuit are [sic:is] hard wired, then the circuit can't be programmable (page 2, section no. 2, second paragraph of the Office Action dated November 15, 2002; paper no. 9).

Because the SOG gate array of New includes logic elements which can be programmed (column 8, lines 36-44), it follows that New does not disclose or suggest one or more logic circuits configured to provide logical operation, wherein the one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), as presently claimed. Therefore, New does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-14 and 17-24 depend, either directly or indirectly, from claims 1 and 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 6 under 35 U.S.C. §103(a) as being unpatentable over New '834 is respectfully traversed and should be withdrawn.

For the reasons presented above, New does not disclose or suggest each and every element of the presently pending claim 1. Specifically, New does not disclose or suggest non-programmable hard wired blocks, as presently claimed. Therefore, presently pending claim 1 is fully patentable over New. Claim 6 depends directly from claim 1 which is believed to be allowable. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

TELEPHONE INTERVIEW

In telephone interviews on July 12, 2003 and July 15, 2003, between Applicant's representative (Robert M. Miller) and Examiner Tran, the independent claims and U.S. Patent No. 5,874,834 to New were discussed. Specifically, Applicant's representative traversed the interpretation of the Sea-of-Gates (SOG) gate array of New as anticipating a non-programmable logic element. No agreement was reached.

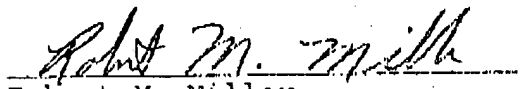
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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